FIG. 1

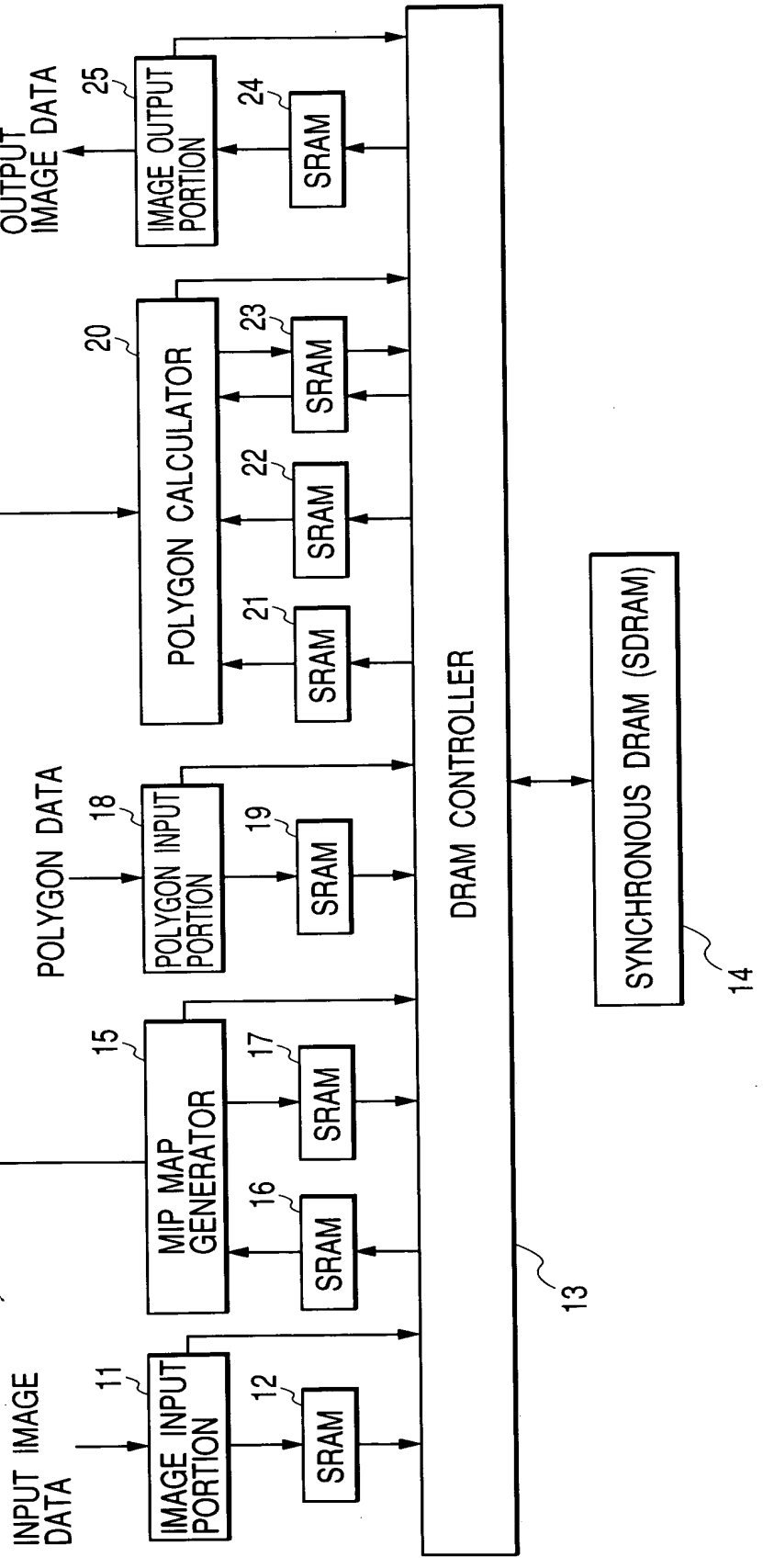

INPUT IMAGE DATA
11
IMAGE INPUT PORTION
12
SRAM
MIP MAP MAXIMUM LEVEL
15
MIP MAP GENERATOR
16
SRAM
17
SRAM
POLYGON DATA
18
POLYGON INPUT PORTION
19
SRAM
20
POLYGON CALCULATOR
21
SRAM
22
SRAM
23
SRAM
OUTPUT IMAGE DATA
25
IMAGE OUTPUT PORTION
24
SRAM
DRAM CONTROLLER
13
SYNCHRONOUS DRAM (SDRAM)
14

FIG. 2

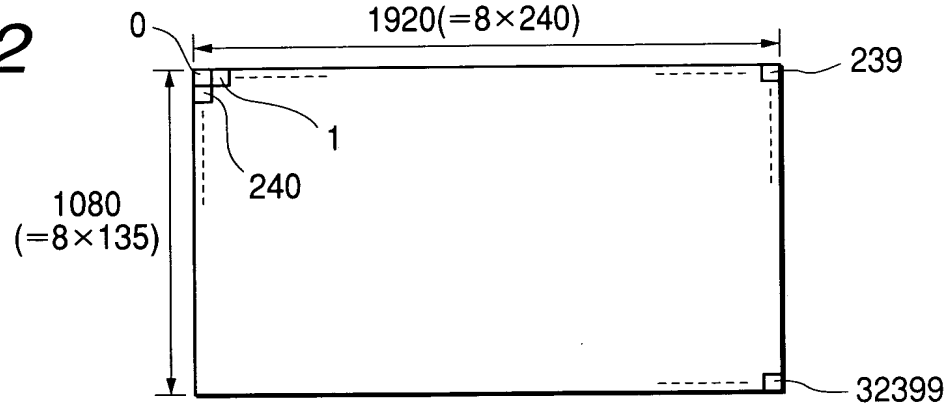



FIG. 3

RESOLUTION L0
(ORIGINAL IMAGE)

X →
Y ↓

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 |
| 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 |
| 16 | 17 | 18 | 19 | 20 | 21 | 22 | 23 |
| 24 | 25 | 26 | 27 | 28 | 29 | 30 | 31 |
| 32 | 33 | 34 | 35 | 36 | 37 | 38 | 39 |
| 40 | 41 | 42 | 43 | 44 | 45 | 46 | 47 |
| 48 | 49 | 50 | 51 | 52 | 53 | 54 | 55 |
| 56 | 57 | 58 | 59 | 60 | 61 | 62 | 63 |

FIG. 4

RESOLUTION L1
(HALF OF ORIGINAL-IMAGE RESOLUTION L0)

X →
Y ↓

| | | | |
|---|---|---|---|
| 0 | 1 | 2 | 3 |
| 4 | 5 | 6 | 7 |
| 8 | 9 | 10 | 11 |
| 12 | 13 | 14 | 15 |

FIG. 5

RESOLUTION L2
(ONE FOURTH OF ORIGINAL-IMAGE RESOLUTION L0)

X →
Y ↓

| | |
|---|---|
| 0 | 1 |
| 2 | 3 |

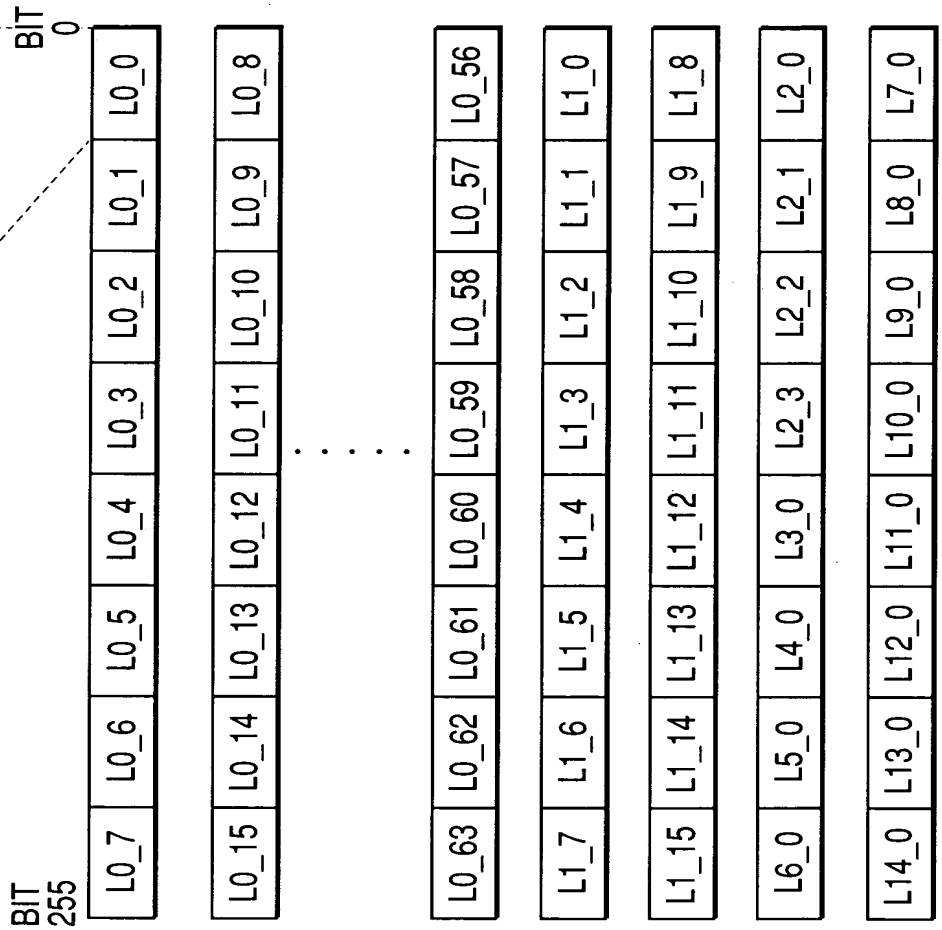
FIG. 6

RESOLUTION L3
(ONE EIGHTH OF ORIGINAL-IMAGE RESOLUTION L0)

X →
Y ↓

| |
|---|
| 0 |

FIG. 7


BIT 31
BIT 0
A B G R
BIT 255
BIT 0
DRAM AD
L0_7 L0_6 L0_5 L0_4 L0_3 L0_2 L0_1 L0_0
DRAM AD+1
L0_15 L0_14 L0_13 L0_12 L0_11 L0_10 L0_9 L0_8
DRAM AD+7
L0_63 L0_62 L0_61 L0_60 L0_59 L0_58 L0_57 L0_56
DRAM AD+8
L1_7 L1_6 L1_5 L1_4 L1_3 L1_2 L1_1 L1_0
DRAM AD+9
L1_15 L1_14 L1_13 L1_12 L1_11 L1_10 L1_9 L1_8
DRAM AD+10
L6_0 L5_0 L4_0 L3_0 L2_3 L2_2 L2_1 L2_0
DRAM AD+11
L14_0 L13_0 L12_0 L11_0 L10_0 L9_0 L8_0 L7_0